#### CSC 370 – Computer Architecture and Organization

Lecture 9 – IA-32 Architecture

#### The Intel Microprocessor Family

- The Intel family owes its origins to the *8080*, an 8-bit processor which could only access 64 kilobytes of memory.
- The *8086* (1978) had 16-bit registers, a 16-bit data bus, 20bit memory using segmented memory. The IBM PC used the *8088*, which was identical except it used an 8-bit data bus.
- *8087* a math co-processor that worked together with the 8086/8088. Without it, floating point arithmetic require complex software routines.
- *80286* ran in real mode (like the 8086/8088) or in protected mode could access up tp 16MB using 24-bit addressing with a clock speed between 12 and 25 MHz. Its math co-processor was the 80287.



- 80386 or *i386* (1985) used 32-bit registers and a 32-bit data bus. It could operate in real, protected or virtual mode. In virtual mode, multiple real-mode programs could be run.
- *i486* The instruction set was implemented with up to 5 instructions fetched and decoded at once. SX version had its FPU disabled.
- The Pentium processor had an original clock speed of 90 MHz and cold decode and executed two instructions at the same time, using *dual pipelining*.



#### IA-32 Processor Address Space

- In protected mode IA-32 processors can access up to 4 Gigabytes of storage, with memory addresses from 0 to 2<sup>32</sup>-1.
- In real mode, a maximum of 1 megabyte of memory can be accessed with memory addresses from 0 to 2<sup>20</sup>-1.
- The IA-32 processors provide a Virtual 8086 where multiple MS-DOS programs can run safely within an Windows environment.



# **CISC** Architecture

- The Intel processors have been based on the CISC (*C*omplex *I*nstruction *S*et *C*omputer) approach to processor design.
- CISC processors have large, powerful instruction sets that can include many high-level operations. But the size of the instruction set makes the control unit relatively slow.



	22.1	
	32-bi	it Register
	General Purpose	Index
3	31 0	
EAX	AX	EBP
EBX	BX	ESP
ECX	СХ	ESI
EDX	DX	EDI
		Segment
	Status and Control	CS
EFLAGS	Flags	SS
ſ		DS
EIP	IP	ES
		FS
		GS





In	ndex Registers
Index Registers co	ntain the offsets for data and
<u>Offset</u> - distance (in segment. BP	BP (Base Pointer) - contains an assumed offset from the SS register; used to locate
SP	SP (Stack Pointer) - contains the offset for the top of the stack.
SI	SI (Source Index) - Points to the source string in string move instructions.
DI	DI (Destination Index) - Points to the source destination in string move

Status an	d Cont	trol R	leg	iste	ers			
IP	IP (Instructure) the next in current co	ction Po nstructio ode segn	inter on to nent.	r) - c be e	onta execu	ins tl ited	he of with	fset of in the
x x x x O D	I T	S Z	x	А	x	Р	x	С
Flags register contains status or arithmetic specific instructions	in indivic results. 7 5.	dual bit They a	ts w re u	hicl sua	h in lly s	dica set b	ite C y	CPU
O = Overflow	S	= Sign						
D = Direction	Z	= Zero						
I = Interrupt	А	= Auxil	iary	Carr	у			
T = Trap	P	= Parity						
x = undefined	С	= Carry						

	Flags
There how repo	are two types of flags: control flags (which determine instructions are carried out) and status flags (which ort on the results of operations.
Contro	l flags include:
— 1 1	<b>Direction</b> Flag (DF) - affects the direction of block data ransfers (like long character string). $1 = up; 0 - down$ .
- 1 0 0 2	<b>Interrupt</b> Flag (IF) - determines whether interrupts can occur (whether hardware devices like the keyboard, disk drives, and system clock can get the CPU's attention to get their needs attended to.
- 2	<i>Trap</i> Flag (TF) - determines whether the CPU is halted after every instruction. Used for debugging purposes.

#### Status Flags

- Status Flags include:
  - *Carry* Flag (CF) set when the result of **unsigned** arithmetic is too large to fit in the destination. 1 = carry; 0 = no carry.
  - Overflow Flag (OF) set when the result of signed arithmetic is too large to fit in the destination. 1 = overflow; 0 = no overflow.
  - Sign Flag (SF) set when an arithmetic or logical operation generates a negative result. 1 = negative; 0 = positive.
  - Zero Flag (ZF) set when an arithmetic or logical operation generates a result of zero. Used primarily in jump and loop operations. 1 =zero; 0 = not zero.
  - Auxiliary Carry Flag set when an operation causes a carry from bit 3 to 4 or borrow (frombit 4 to 3). 1 = carry, 0 = no carry.
  - *Parity* used to verify memory integrity. Even # of 1s = Even parity; Odd # of 1s = Odd Parity











### Paging

- IA-32 architecture also allows memory segments to be divided into 4K units called *pages*.
- Many of these pages of memory are saved on disk in a swap file and are loaded into memory (and rewritten in the swap file) when the CPU needs a page that is not present in physical memory. This situation is called a *page fault*.
- The use of paging and swap files allows the memory used to be several times larger than physical memory; it is known as *virtual memory*.



Expression	Value	]
16 / 5	3	1
- (3 + 4) * (6 - 1)	-35	1
-3 + 4 * 6 - 1	20	]
4 + 5 * 2	1	
-5 + 2		
12 - 1 MOD 5		1
(4 + 2) * 6		







#### **Reserved Words**

- Reserved words have a special meaning to the assembler and cannot be used for anything other than their specified purpose.
- They include:
  - Instruction mnemonics
  - Directives
  - Operators in constant expressions
  - Predefined symbols such as @data which return constant values at assembly time.

Examp	ples of Identifiers
var1 _main @@myfile Count xVal	open_file _12345 \$first MAX























Type	Usage
BYTE	8-bit unsigned integer
SBYTE	8-bit signed integer
WORD	16-bit unsigned integer; also Near Pointer in Real Mode
SWORD	16-bit signed integer
DWORD	32-bit unsigned integer; also Near pointer in Protected Mode
SDWORD	32-bit signed integer









Examples o	of Rea	al Da	ta Definitions
rVal1	REAL	4	-2.1
rVal2	REAL	8	3.2E-260
rVal3	REAL	10	4.6E+4096
ShortArray	REAL	4	20 DUP(?)
rVal1	DD	-1.2	
rVal2	dq	3.2E	-260
rVal3	dt	4.6E	+4096

Rang	ges For R	eal Numbers
<u>Data Type</u>	Significant Digits	<u>Approximate Range</u>
Short Real	6	1.18×10 <sup>-38</sup> to 3.40×10 <sup>38</sup>
Long Real	15	2.23×10 <sup>-308</sup> to 1.79×10 <sup>308</sup>
Extended Real	19	3.37×10 <sup>-4932</sup> to 1.18×10 <sup>4932</sup>





```
. code
main PROC
          eax, val1 ; Start with 10000h
 mov
          eax, val2 ; Add 40000h
  add
          eax, val3 ; Subtract 2000h
  sub
  mov
          finalVal, eax ; Save it
  call
          DumpRegs ; Display the
                    ; registers
  exit
main ENDP
  end
          main
```





mov I	nstruction Examples
Examples of mov in	structions
.data	
Count BYTE	10
Total WORD	4126h
Bigval DWORD	12345678h
.code mov al, bl mov bl, count mov count, 26 mov bl, 1 mov dx, cx mov bx, 8FE2h	<pre>; 8-bit register to register ; 8-bit memory to register ; 8-bit immediate to memory ; 8-bit immediate to register ; 16-bit register to register ; 16-bit immediate to register</pre>
mov eax, ebx	; 32-bit register to register
mov edx, bigVal	; 32-bit memory to register

# Arithmetic Instructions

Assembly language include many instructions to perform basic arithmetic. They include:

- inc
- dec
- add
- sub

















```
Implementing Arithmetic Expressions (continued)
; second term: (Yval - Zval)
    mov ebx, Yval
    sub ebx, Zval ; EBX = -10
; add the terms and store
    add eax, ebx
    mov Rval, eax ; Rval = -36
```

#### **Indirect Operands**

- An indirect operand is a register containing the offset for data in a memory location.
  - The register points to a label by placing its offset in that register
  - This is very convenient when working with arrays; it is just a matter of incrementing the address so that it points to the next array element.
  - The ESI, EDI, EBX, EBP, SI, DI, BX and BP registers can be used for indirect operands as well as the 32-bit general purpose registers (with a restriction on the ESP).



```
Indirect Operands: A Protected Mode Example
.data
val1 BYTE 10h
. code
            esi
                 OFFSET val1
     mov
                             ; AL = 10h
            al, [esi]
     mov
            [esi], bl
                      ; The variable to
     mov
                       ; which ESI points is
                       ; changed
     mov
            esi, O
                       ; General Protection
      mov
           ax, [esi]
                        ; Error
            [esi] ; Error - needs size
      inc
           byte ptr [esi] ; Works!
      inc
```







#### Indexed Operands – An Example

```
.data
          BYTE 10h, 20h, 30h
arrayB
          WORD 1000h, 2000h, 3000h
arrayW
. code
          esi, O
     mov
          al, [arrayB+esi] ; AL = 10h
     mov
           esi, OFFSET arrayW
     mov
          ax, [esi] ; AX = 1000h
     mov
          ax, [esi+2] ; AX = 2000h
     mov
           ax, [esi+4]
                          ; AX = 3000h
     mov
```









```
L1:

add ax, [edi] ; add an integer

add edi, TYPE intarray; point to next integer

loop L1 ; repeat ECX = 0

call DumpRegs

exit

main endp

end main
```



# Runtime Stack

- The runtime stack is a memory array that is managed directly by the CPU using the SS and ESP registers.
- In Protected mode, the SS register holds a segment descriptor and is not modified byu user programs; the ESP register holds a 32-bit offset into some memory location on the stack.















#### Procedures

- In general, there are two types of subprograms: functions and procedures (or subroutines).
  - *Functions* return a value (or *result*).
  - <u>Procedures</u> (or <u>subroutines</u>) do not.
  - The terms procedures and subroutines are used interchangeably although some languages use one term and others use the other.
  - Calling a procedure implies that there is a return. Also implies is that the state of the program, (register values, etc.) are left unaffected when the program returns to the calling procedure or program.





F	Passing Pa	rameters	
Passing argument	ts in register	8	
<ul> <li>The most con between the c procedures th</li> </ul>	nmon methoc calling progra at it calls is t	l for passing parameter m (or procedure) and the hrough the registers	
<ul> <li>It is efficient immediate an registers are f</li> </ul>	because the c d direct use c aster than me	alled procedure has of the parameters and emory.	
– Example: Wr	iteInt		
.data		224	
.code	DWORD	234	
	mov	eax, aNumber	
	call	WriteInt	





```
Procedure ArraySum
ArraySum PROC
;------
; Calculates the sum of an array of 32-bit integers.
; Receives: ESI - the array offset
          ECX = # of elements in array
;
; Returns EAX - the sum of the array
;-----
                    ; save ESI, ECX
 push
          esi
 push
          ecx
                    ; Sum = 0
 mov
          eax, O
        eax, [esi] ; Sum = Sum + x[i]
L1:add
                   ; Point to next integer
  add
         esi, 4
          L1
                    ; Repeat for array size
 loop
          ecx
  pop
          esi
  pop
  ret
ArraySum ENDP
```

```
Calling ArraySum
TITLE Driver for Array Sum
                             (ArrayDr.asm)
           Irvine32.inc
INCLUDE
.data
           DWORD 10000h, 20000h, 30000h, 40000h
array
theSum
           DWORD ?
. code
main PROC
          esi, OFFSET array ; ESI points to array
 mov
          ecx, LENGTHOF array ;ECX = array count
  mov
          ArraySum ; calculate the sum
  call
  mov
           theSum, eax
                           ; returned in EAX
                            ; Is it correct?
  call
           WriteHex
  exit
main ENDP
ArraySum PROC... ... Procedure goes here
  END main
```



CMP Results		
CMP Results	ZF	<u>CF</u>
destination < source	0	1
destination > source	0	0
destination = source	1	0

CMP Re	esults
CMP Results	Flags
destination < source	SF ≠ OF
destination > source	SF = OF
destination = source	ZF = 1











#### Jcond Instruction

- A conditional jump instruction branches to a destination label when a flag condition is true.
- If the flag is false, the instruction immediately following the conditional jump is performed instead.
- The syntax is: Jcond destination



```
Examples of Conditional Jumps
• In all three cases, the jump is made:
      mov
           ax, 5
      cmp
           ax, 5
           L1 ; jump if equal
      je
           ax, 5
      mov
           ax, 6
      cmp
      jl
           L1
               ; jump if less
      mov
           ax, 5
           ax, 4 ; jump if greater
      cmp
```

Jumps Da	sed on General C	20111120115
Mnemonic	Description	Flags/Registers
JZ	Jump if zero	ZF = 1
JE	Jump if equal	ZF = 1
JNZ	Jump if not zero	ZF = 0
JNE	Jump if not equal	ZF = 0

Mnenomic	Description	Flags/Registers
JC	Jump if carry	CF = 1
JNC	Jump if not carry	CF = 0
JCXZ	Jump if CX = 0	CX = 0
JECXZ	Jump if ECX = 0	ECX = 0

### Jumps based on General Comparisons

Mnenomic	Description	Flags/Registers
JP	Jump if Parity even	PF = 1
JNP	Jump if Parity odd	PF = 0

Mnenomic	Description	Flag(s)
JA	Jump if above (op1 > op2)	CF = 0 & ZF = 0
JNBE	Jump if not below or equal	CF = 0 & ZF = 0
JAE	Jump if above or equal	CF = 0
JNB	Jump if not below	CF = 0

# Jumps based on Unsigned Comparisons

Mnenomic	Description	Flag(s)
JB	Jump if below (op1 < op2)	CF = 1
JNAE	Jump if not above	CF = 1
JBE	Jump if below or equal	CF = 1  or  ZF = 1
JNA	Jump if not above	CF = 1  or  ZF = 1

٠. ١		
Mnenomic	Description	Flag(s)
JG	Jump if greater	SF = 0 & ZF = 0
JNLE	Jump if not less	SF = 0 & ZF =0
	than or equal	
	In the second	
JGE	than or equal	SF = OF
JNL	Jump if not less	SF = OF
	than	

Mnenomic	Description	Flag(s)
JL	Jump if less	SF <> OF
JNGE	Jump if not greater than or equal	SF <> OF
JLE	Jump if less than or	ZF = 1  or
	equal	SF = <> OF
JNG	Jump if not greater	ZF = 1  or
	than	SF = <> OF

Mnenomic	Description	Flag(s)
JS	Jump if signed (op1 is negative)	SF = 1
JNS	Jump if not signed	SF = 0
JO	Jump if overflow	OF = 1
JNO	Jump if not overflow	OF = 0













- The **IMUL** instruction sets the Carry and Overflow flags if the upper half of the product is not a sign extension of the low-order product.equal to zero.
- E.g., if AX is multiplied by a 16-bit multiplier, the product is stored in DX:AX. IF the AX contains a negative value and the DX is not all 1s, the Carry and Overflow flags are set.

-	<b>IMUL</b> Instruction - Examples
• 8-bit signed	ed multiplication (48 * 4)
mov	al, 48
mov	bl, 4
imul	bl ; $AX = 00C0h$ , $OF = 1$
• 16-bit sign	ned multiplication (-4 * 4)
mov	al, -4
mov	bl, 4
imul	bl ; $AX = FFF0h$ , $OF = 0$
• 32-bit sign	ned multiplication (12345h*1000h)
mov	eax, +4823424
mov	ebx, -423
imul	ebx ; EDX:EAX =
	; FFFFFFF86636D80h, OF = $0$





# .data byteVal SBYTE -48 .code mov al, byteVal ; dividend cbw ; extend Al into AH mov bl, 5 ; divisor idiv bl ; AL = -9, AH = -3



# IDIV Instruction - 32-bit Example .data wordVal SWORD -50000 .code mov eax, dwordVal ; dividend, low cdq ; extend EAX into EDX mov ebx, 256 ; divisor idiv bx ; quotient EAX = -195 ; remainder EDX = -80