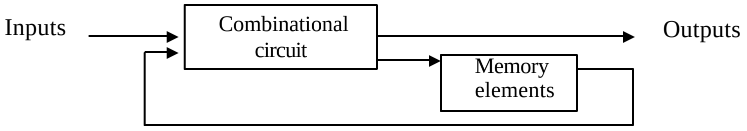
Systems I: Computer Organization and Architecture

Lecture 7: Synchronous Sequential Logic

Synchronous Sequential Logic

- The digital circuits that we have looked at so far are combinational, depending only on the inputs. In practice, most systems have many components that contain memory elements, which require ***sequential*** logic.
- A sequential circuit contains both a combinational circuit and memory elements, whose output also serves as an input for the combinational circuit.
- The binary data stored in the memory elements define the state of the sequential circuit and help determine the conditions for changing the state in the memory elements.



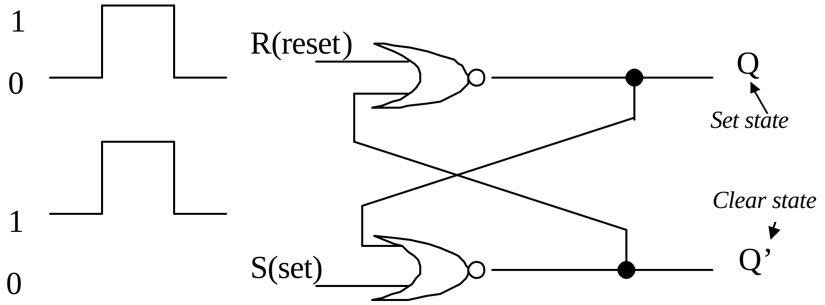
Sequential Circuits: Synchronous and Asynchronous

- There are two types of sequential circuits, classified by their signal's timing:
  - Synchronous sequential circuits have behavior that is defined from knowledge of its signal at discrete instants of time.
  - The behavior of asynchronous sequential circuits depends on the order in which input signals change and are affected at any instant of time.

Synchronous Sequential Circuits

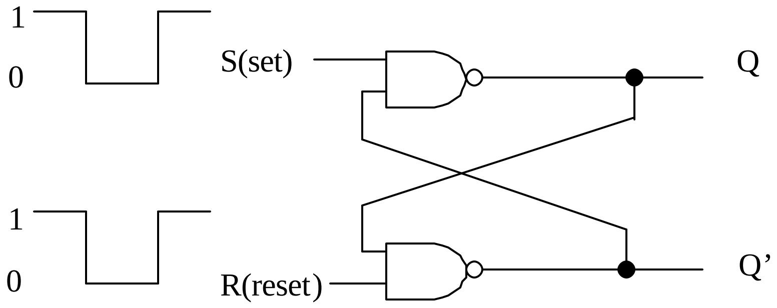
- Synchronous sequential circuits need to use signal that affect memory elements at discrete time instants.
- Synchronization is achieved by a timing device called a master-clock generator which generates a periodic train of clock pulses.

Basic Flip-Flop Circuit Using NOR Gates



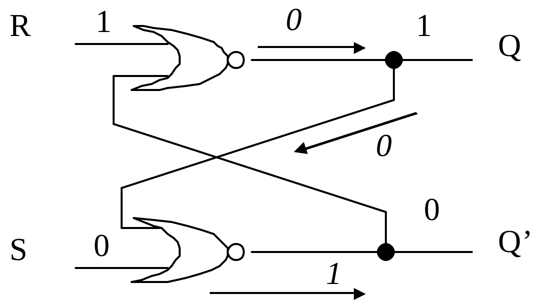
S	R	Q	Q’	
1	0	1	0	
0	0	1	0	(after S = 1, R = 0)
0	1	0	1	
0	0	0	1	(after S = 0, R = 1)
1	1	0	0	

Basic Flip-Flop Circuit Using NAND Gates

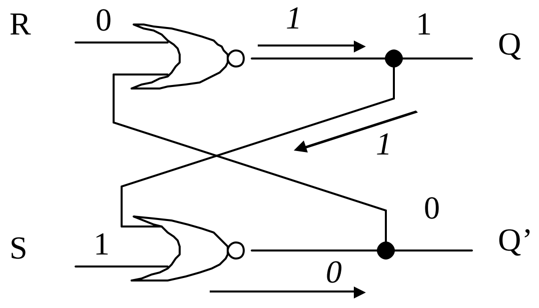


S	R	Q	Q’	
1	0	0	1	
1	1	0	1	(after S = 1, R = 0)
0	1	1	0	
1	1	1	0	(after S = 0, R = 1)
1	1	0	0	

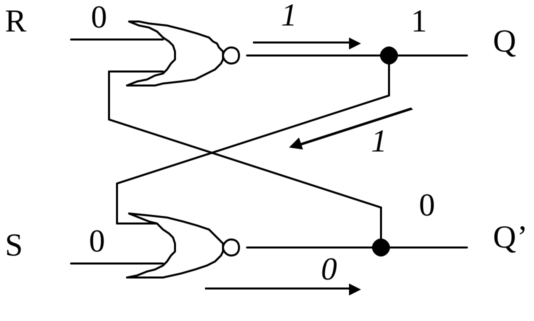
How the Basic Flip-Flop Circuit Works



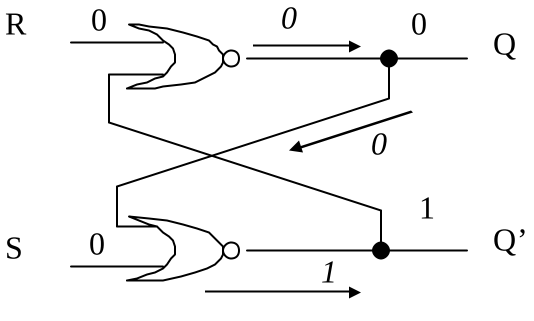
How the Basic Flip-Flop Circuit Works



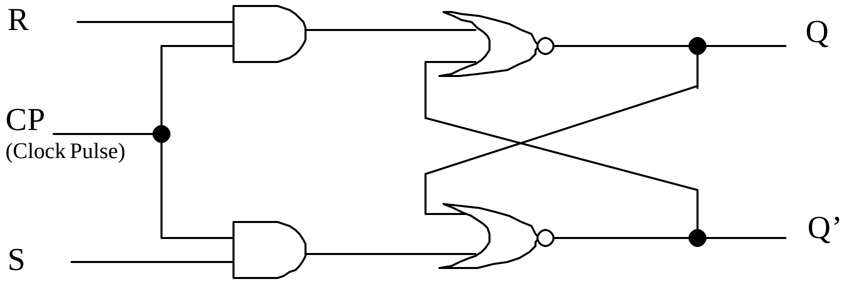
How the Basic Flip-Flop Circuit Works

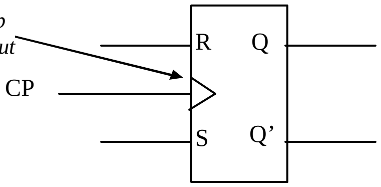


How the Basic Flip-Flop Circuit Works



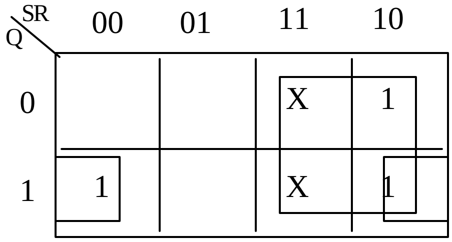
Clocked RS Flip-Flop





Dynamic indicator - denotes that the flip-flop responds to a clock input

Karnaugh Map for Clocked RS Flip-Flop



Q \ SR	00	01	11	10
0			X	1
1	1		X	1

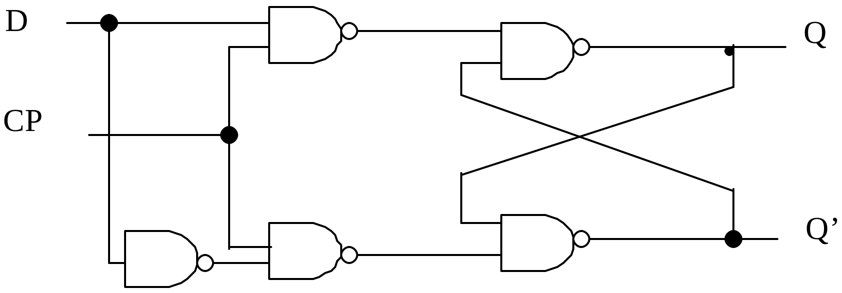
Q(t+1) = S + R’Q(t)

SR = 0

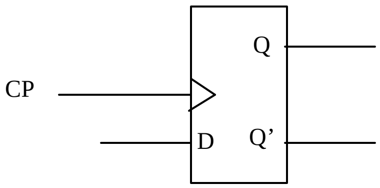
Truth Table for Clocked RS Flip-flop

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

D Flip-Flops



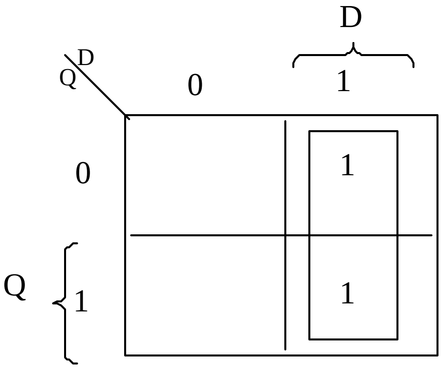
D Flip-flops are a modification of RS flip-flops which Q is set to whatever value D has.



Truth Table for D Flip-flops

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

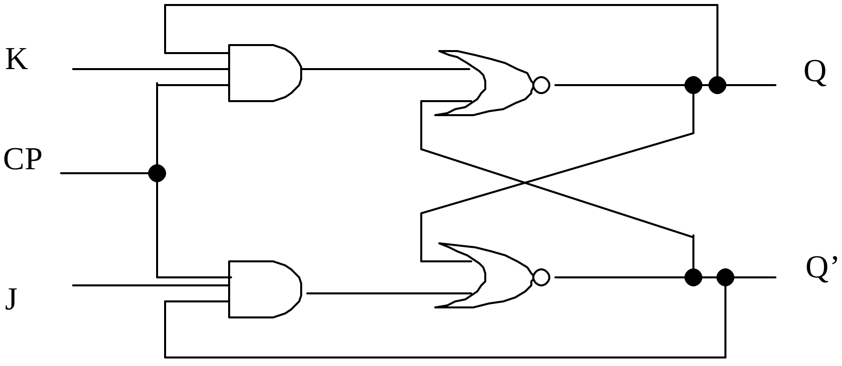
Karnaugh Map for D Flip-flops



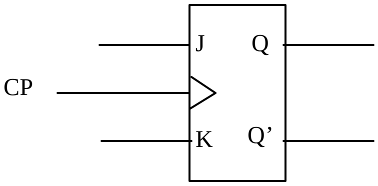
Q \ D	0	1
0		1
1		1

Q(t+1) = D

JK Flip-flops



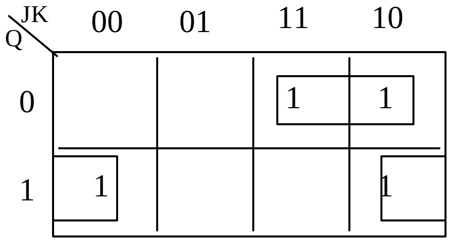
JK Flip-flops are a refinement of RS Flip-flops where the indeterminate state is now a “toggle”



Truth Table for JK Flip-flops

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

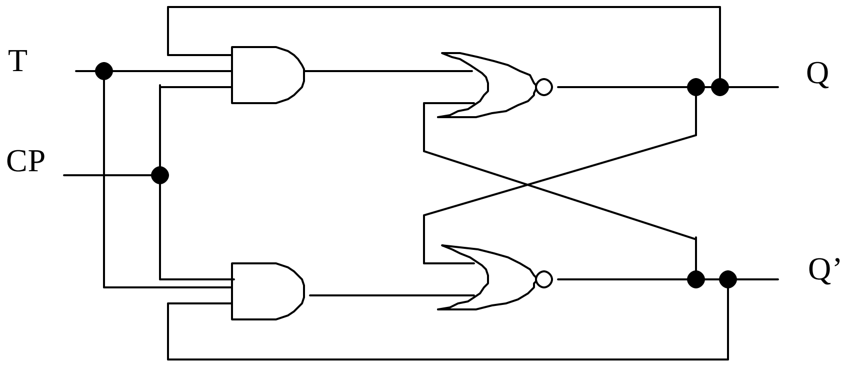
Karnaugh Map for JK Flip-flops



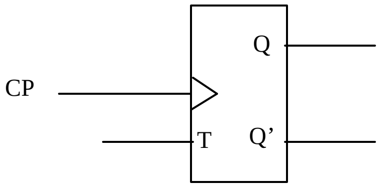
Q \ JK	00	01	11	10
0			1	1
1	1			1

Q(t+1) = JQ’ + K’Q

T Flip-flops



T flip-flops are a single-input version of JK Flip-flops where the input “toggles” the output



Truth Table for T Flip-flops

Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Karnaugh Map for T Flip-flops

			T
	Q \ T	0	1
	0		1
Q	1	1	

Q(t+1) = TQ’ + T’Q

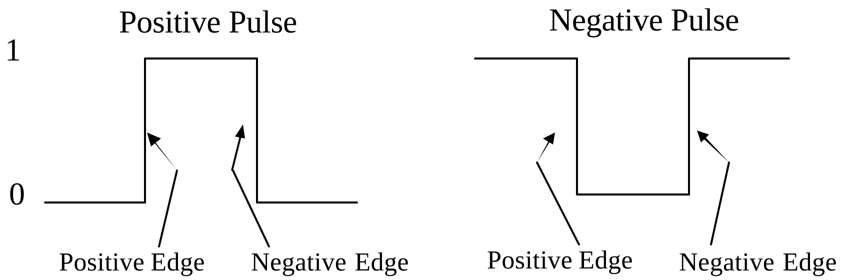
Triggering Flip-flops

- The state of a flip-flop is switched by a momentary change in input signal (called a ***trigger***).
  - RS flip-flops are asynchronous and require an input trigger defined by a change of signal level. If the level does not return to its original level (0 in NOR flip-flops; 1 in NAND flip-flops), they cannot be triggered again.
  - Clocked flip-flops are triggered by pulses, which start at a value of 0, rise to 1 momentarily and return to 0.

Triggering Flip-flops (continued)

- Sequential circuits have feedback paths between the combinational circuits and memory elements, which could produce instability if memory element outputs are changing while combinational circuit outputs are sampled by the clock pulse.
- This timing problem can be solved by not have flip-flop outputs change until the pulse returns to 0. This requires delaying the propagation of the flip-flop's signal.
- This is more easily done by having the delay unit within the flip-flop.

Clock Pulses

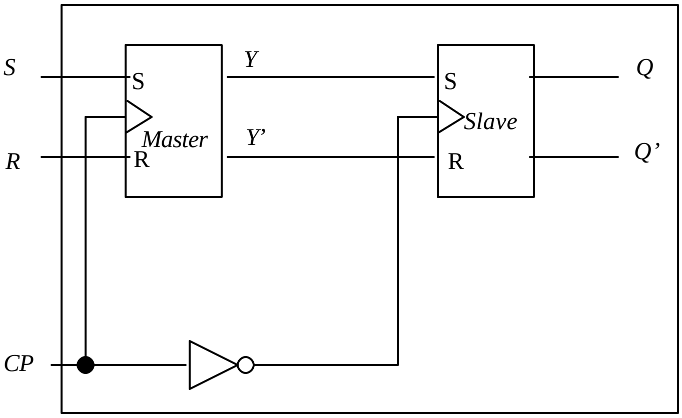


To avoid having a flip-flop change values during the life of a clock pulse, it is important to have the flip-flop respond to either positive ***or*** negative edge ***only***.

Master-Slave Flip-Flop

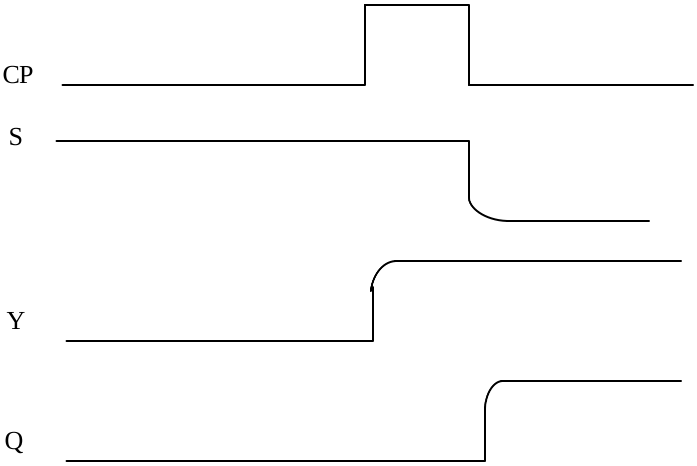
- A master-slave flip-flop consists of two flip-flops, one serving as a master, one serving as a slave and an inverter for the clock pulse.
- First the master is set (or cleared) and then the slave.

Master-Slave Flip-Flop Logic Diagram



Master-Slave Flip- flop

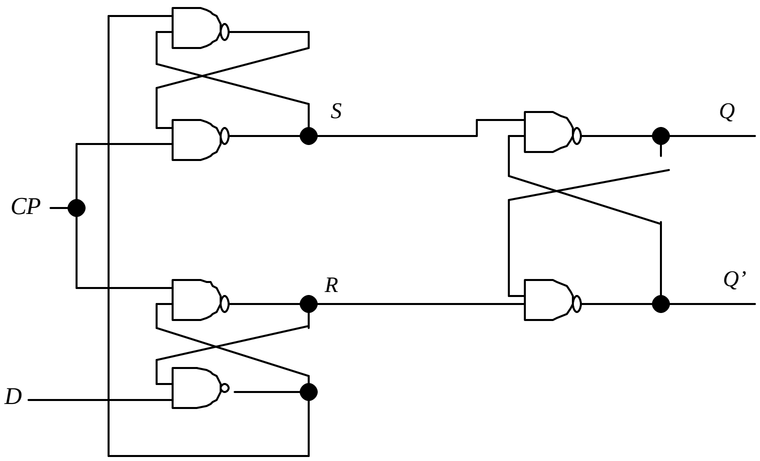
Master-Slave Flip-Flop Timing Relationships



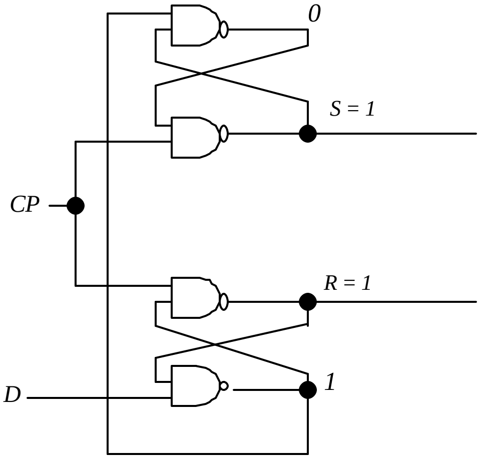
Edge-Triggered Flip-Flops

- In edge-triggered flip-flops, output transitions occur at a specific level of the clock pulse.
- When the pulse exceeds this threshold, inputs are locked out and the flip-flop won't respond to input until the clock pulse returns to 0.
- ***Setup time*** – the time for which the D input must be maintained at a constant value prior to application of the pulse.
- ***Hold time*** – the time for which the D input must not change after the application of the positive-going transition of the pulse.

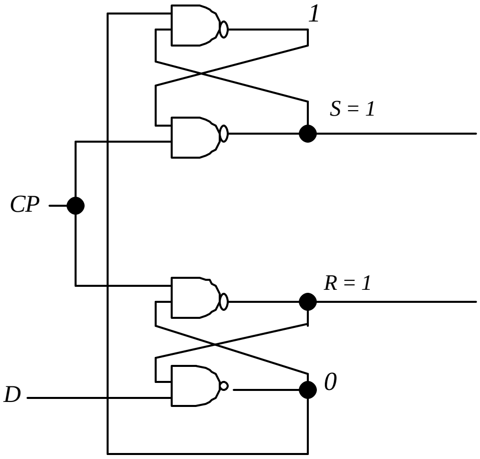
D-type Positive-Edge-Triggered Flip-Flop



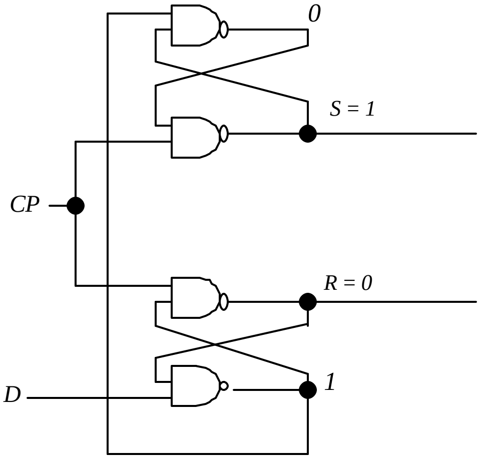
Edge-Triggered With CP= 0 & D = 0



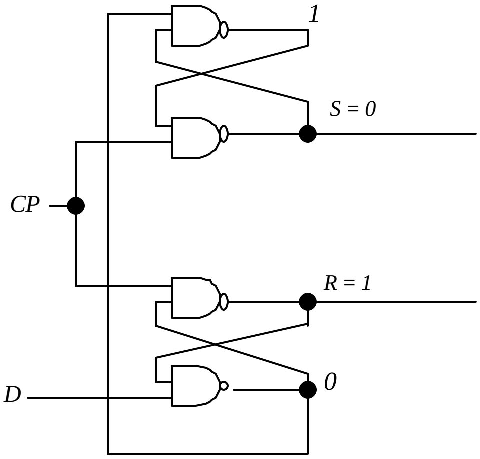
Edge-Triggered With CP= 0 & D = 1



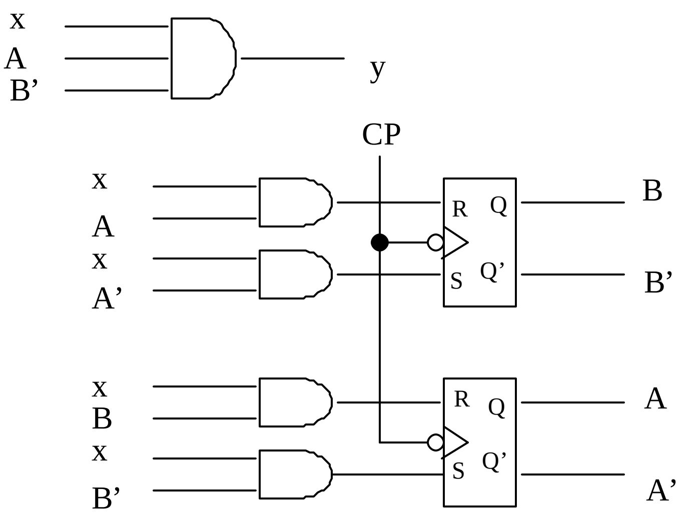
Edge-Triggered With CP= 1 & D = 0



Edge-Triggered With CP= 1 & D = 1



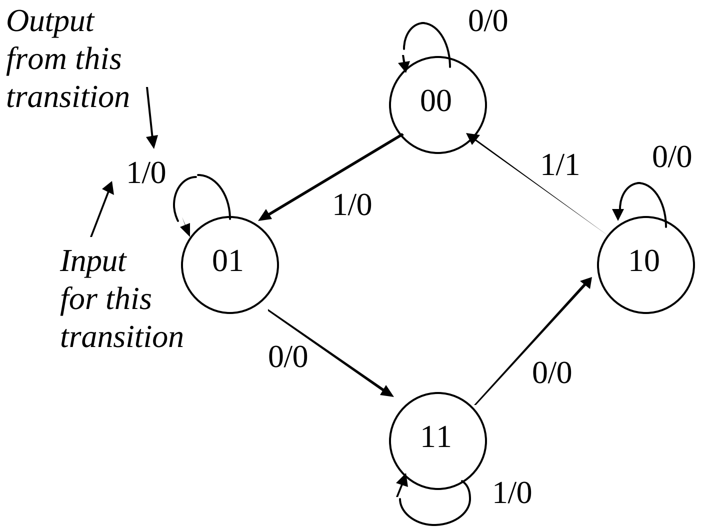
Sequential Circuit – An Example



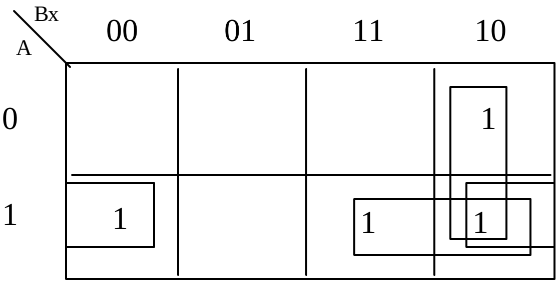
State Table for the Sequential Circuit

	Next state		Output	
Present State	***x = 0***	***x = 1***	***x = 0***	***x = 1***
AB	**AB**	**AB**	**y**	**y**
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	10	11	0	0

State Diagram for the Sequential Circuit



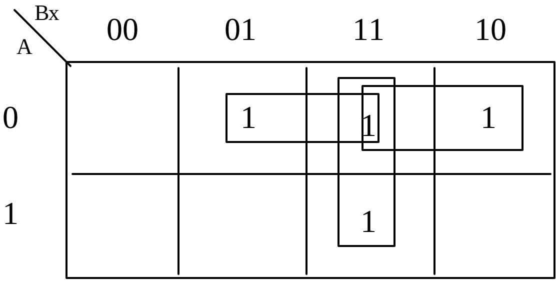
State Equations for the Sequential Circuit



A \ Bx	00	01	11	10
0				1
1	1		1	1

$$\begin{aligned} A(t+1) &= Bx' + (B+x')A \\ &= Bx' + (B'x)'A \end{aligned}$$

State Equations for the Sequential Circuit



A \ Bx	00	01	11	10
0		1	1	1
1			1	

$B(t+1) = A'x + (A'+x)B$

$= Ax + (Ax')'B$

Flip-flop Excitation Tables

- Characteristic tables tell us the state into which a flip-flop goes depending on the inputs.
- What we really want to know is what inputs we need to get the flip-flop to make a particular transition

Characteristic Table for RS Flip-flop

S	**R**	**Q(t+1)**
0	0	Q(t)
0	1	0
1	0	1
1	1	?

Excitation Table for RS Flip-flop

Q(t)	**Q(t+1)**	**S**	**R**
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table for JK Flip-flop

Q(t)	**Q(t+1)**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table for D Flip-flop

Q(t)	**Q(t+1)**	**D**
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table for T Flip-flop

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Sequential Logic Design

- Designing a sequential circuits consits of choosing the flip-flops and combinational gates.
  - The number of flip-flops depends on the number of states in the circuits.
  - The combinational circuit depends on the state table.

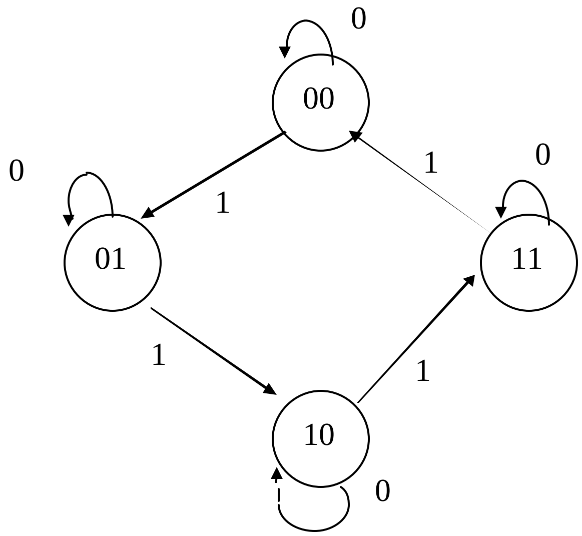
Sequential Logic Design Procedure

- The procedure is summarized by these steps:
  1. The word description of the circuit behavior is states, accompanied by a state diagram, timing diagram or other pertinent data.
  2. Obtain the state table from the given information about the circuit.
  3. The number of states may be reduced if the sequential circuit can be characterized by input-output relationships independent of the number of states.
  4. Assign binary values to each state if the state table obtained in step 2 or 3 contains letter symbols.

Sequential Logic Design Procedure (continued)

5. Determine the number of flip-flops needed and assign a letter symbol to each
6. Choose the type of flip-flop to be used.
7. From the state table, derive the circuit excitation and output table.
8. Using the map or any other simplification method, derive the circuit output function and the flip-flop input functions.
9. Draw the logic diagram.

Example - A Simple Counter



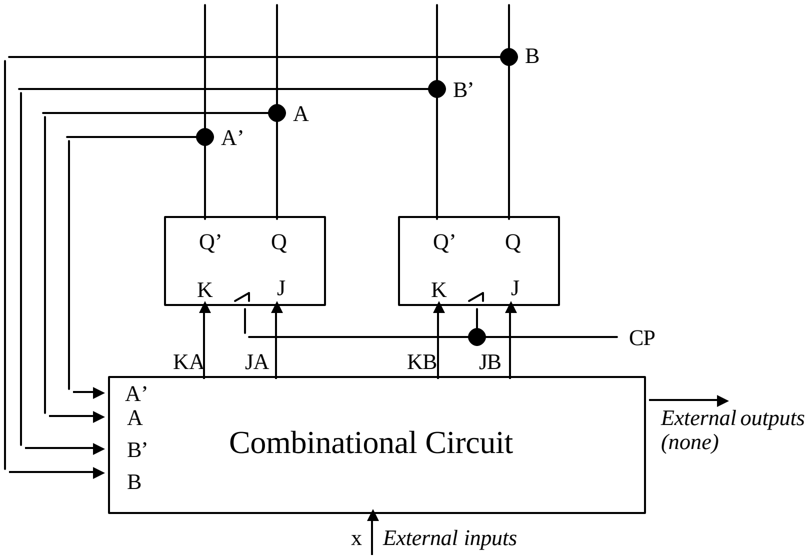
State Table for the Sequential Circuit

Present State		Next State			
		x = 0		x = 1	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	0	1	1	0
1	0	1	0	1	1
1	1	1	1	0	0

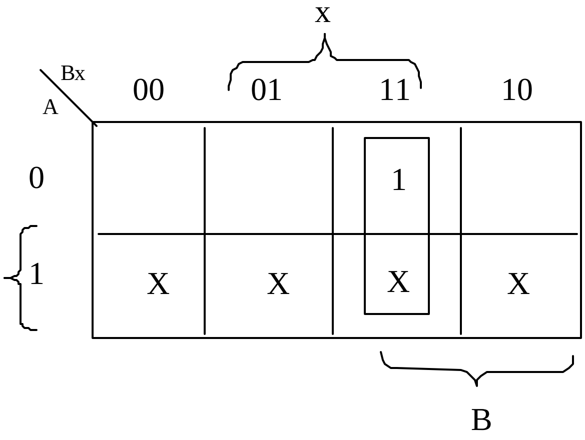
Excitation Table for the Sequential Circuit

Inputs of combinational circuit					Outputs of combinational circuit			
Present State		Input	Next State		Flip-flop inputs			
A	B	x	A	B	JA	KA	JB	KB
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Block Diagram for Sequential Circuit



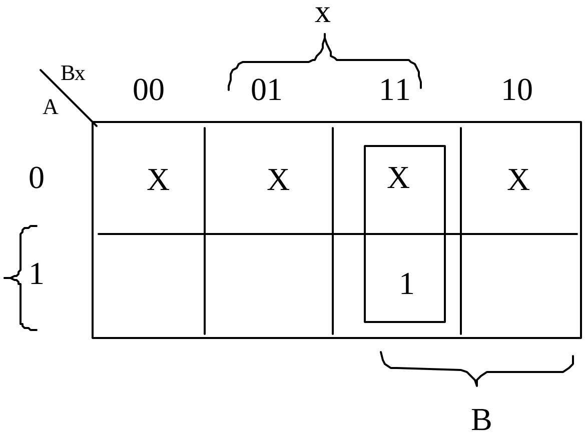
Karnaugh Maps for Combinational Circuit



A \ Bx	00	01	11	10
0			1	
1	X	X	X	X

JA = Bx

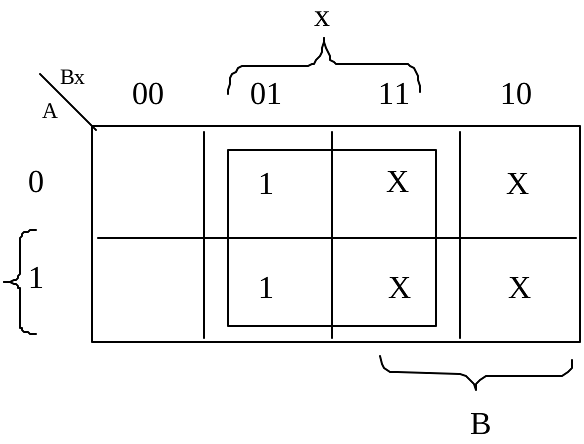
Karnaugh Maps for Combinational Circuit (continued)



A \ Bx	00	01	11	10
0	X	X	X	X
1			1	

KA = Bx

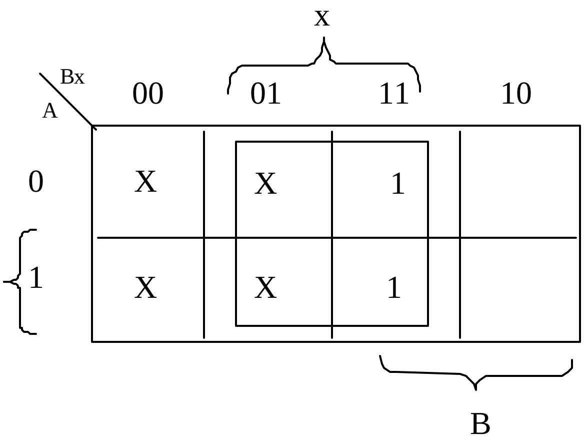
Karnaugh Maps for Combinational Circuit (continued)



A \ Bx	00	01	11	10
0		1	X	X
1		1	X	X

JB = x

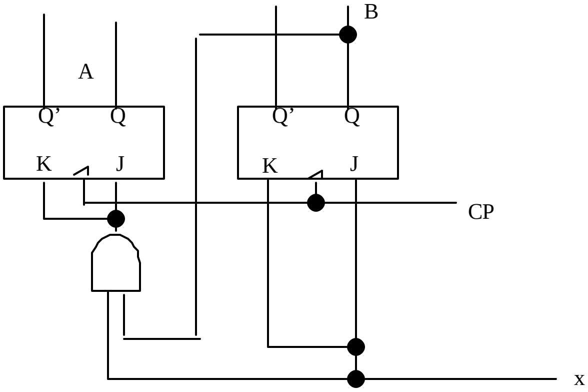
Karnaugh Maps for Combinational Circuit (continued)



A \ Bx	00	01	11	10
0	X	X	1	
1	X	X	1	

KB = x

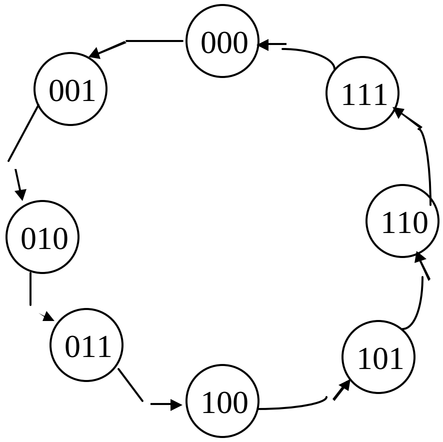
Circuit Diagram for Sequential Circuit



Designing a Binary Counter

- A sequential circuit that goes through a prescribed sequence of states when an input pulse is applied is called a ***counter***.
- The straight binary sequence is the simplest sequence and a counter that follows it is called a ***binary counter***.
- An binary counter with n flip-flops will count from 0 to 2^n-1.

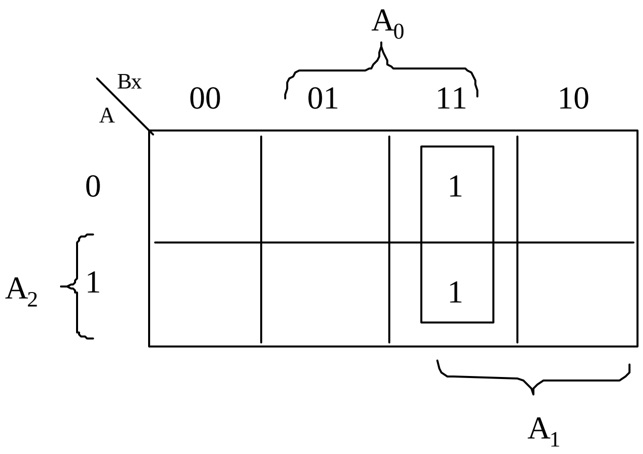
State Diagram for a Binary Counter



Excitation Table for 3-bit Binary Counter

Count Sequence			Flip-flop inputs		
A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	1	1	1

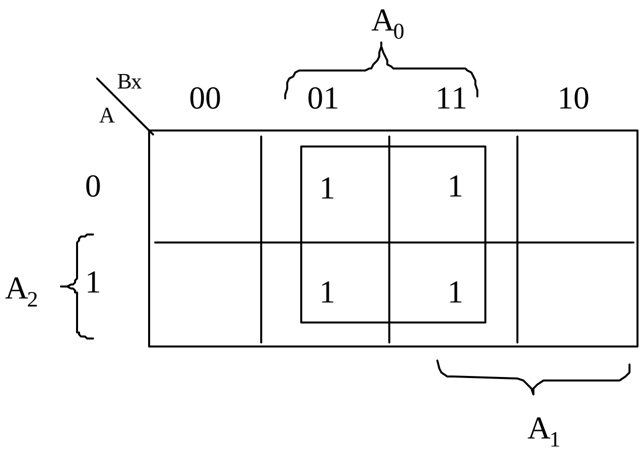
Karnaugh Maps for Binary Counter



A \ Bx	00	01	11	10
0			1	
1			1	

$TA_2 = A_1A_0$

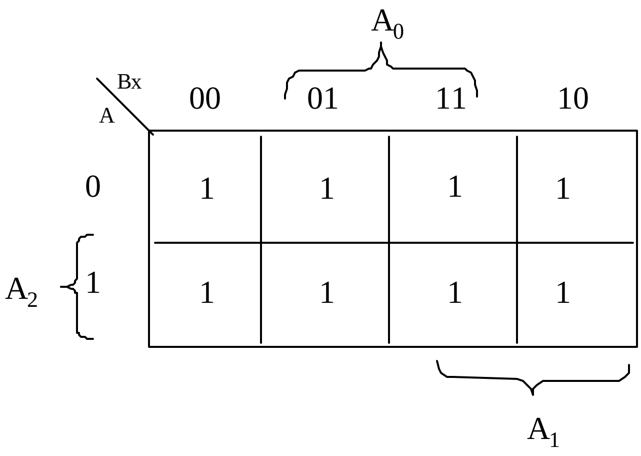
Karnaugh Maps for Binary Counter (continued)



A \ Bx	00	01	11	10
0		1	1	
1		1	1	

$TA_1 = A_0$

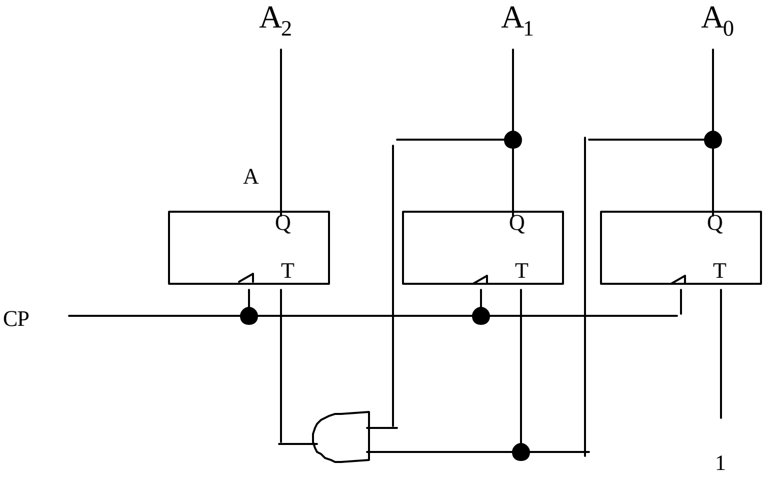
Karnaugh Maps for Binary Counter (continued)



A \ Bx	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$TA_0 = 1$

Circuit Diagram for Binary Counter



A_2
A_1
A_0
A
Q
Q
Q
T
T
T
CP
1